Amendments to the Specification

Please **replace** the paragraph beginning at page 1, line 3 (under the heading "Cross Reference to Related Applications") with the following **amended** paragraph:

-- This patent application is related to simultaneously filed U.S. Patent Application No. ~~XXXXXX~~10/055,114, filed ~~XXXX~~January 23, 2002 (Attorney Docket No. PU020002) entitled INTRA-DECODER COMPONENT BLOCK MESSAGING; and U.S. Patent Application No. ~~XXXXXX~~10/055,470, filed ~~XXXX~~January 23, 2002 (Attorney Docket No. PU020001) entitled CHIEN SEARCH CELL FOR AN ERROR-CORRECTING DECODER, both of which are incorporated herein by reference in their entireties. --

Please **replace** the paragraph beginning at page 1, line 26 with the following **amended** paragraph:

-- One frequently used scheme for error detection/correction is through the use of so-called Reed-Solomon codes. Reed-Solomon codes are non-binary systematic cyclic linear block codes. Non-binary codes work with symbols that are comprised of several bits. Non-binary ~~code~~ codes, such as the Reed-Solomon code, are good at correcting burst errors because the correction by these codes is done on the symbol level. A systematic code, such as the Reed-Solomon code, generates codewords that contain the message symbols in unaltered form. The encoder applies a reversible mathematical function to the message symbols in order to generate the redundancy, or parity, symbols. The codeword is then formed by appending the parity symbols to the message symbols. The Reed-Solomon code is considered a ~~cyclical~~ cyclic code because a circular shift of any valid codeword also produces another valid codeword. Cyclic codes are popular because there exist efficient and inexpensive decoding techniques to implement them.

Finally, the Reed-Solomon code is considered linear because the addition of any two valid codewords results in another valid codeword. --

Please **replace** the paragraph beginning at page 2, line 8 with the following **amended** paragraph:

-- A typical Reed-Solomon decoder is comprised of the following major component blocks: (*i*) a syndrome generating block, (*ii*) an error polynomial block, (*iii*) an error location block, and (*iv*) an error magnitude block, (*v*) an error correcting block, and (*vi*) a delay block. The syndrome generating block is used to ~~receive a codeword and~~ generate a syndrome from the ~~codeword~~ received codeword data. The syndrome is utilized to create an error polynomial in the error polynomial block. The error polynomial is passed onto the error location and error magnitude blocks, in which error locations and magnitudes for a codeword are respectively determined. An error vector is generated from the error location and magnitude. A delayed version of the received codeword data is corrected by the error correcting block using the error vector corresponding to a specific codeword. --

Please **replace** the paragraph beginning at page 2, line 21 with the following **amended** paragraph:

-- The present invention is a method and an apparatus for error location and magnitude determination of ~~a codeword~~ received codeword data by a decoder. A value corresponding to the number of codeword errors is calculated. Should the value corresponding to the number of ~~codeword~~ received codeword data errors be greater than a threshold value, the ~~codeword~~ received codeword data is forwarded as the output of the decoder. Should the value

corresponding to the number of ~~codeword~~ received codeword data errors be less than or equal to the threshold value, then ~~determine~~ the error locations and the error magnitudes corresponding to the ~~codeword~~ received codeword data are determined. The present invention is characterized in that the act of calculating the value corresponding to the number of codeword errors is performed on data corresponding to a first codeword while the act of determining the error locations and the error magnitudes is concurrently performed on data corresponding to a second codeword. --

Please **replace** the paragraph beginning at page 4, line 32 with the following **amended** paragraph:

-- With reference to Fig. 2, there is depicted a flow chart illustrating the various error detecting/correcting processes available within the context of a transmitter/channel/receiver environment. Although described in such a context, it would be apparent to those skilled in the art that such error detecting/correcting processes would also apply equally to broadcast transmission, digital data storage, or any other process in which digital data (whether in the form of a data field, packet, stream, etc.) is processed or manipulated. By way of example, merely illustrative and not meant to be exhaustive or exclusive, the following technologies/devices may utilize error detection/correction schemes to improve performance, integrity, and reliability: (*i*) various storage ~~devices, including but not limited to tape,~~ devices including, but not limited to, tape, compact disc (CD), digital versatile disc (DVD), barcodes, etc., (*ii*) wireless or mobile communications (including cellular telephones, two way transceivers,

microwave links, etc., (*iii*) satellite communications, (*iv*) digital radio, digital television (DTV), digital video broadcasting (DVB), etc., (*v*) modems, including but not limited to cable, V.pcm, ADSL, xDSL, etc. --